REMARKS

The Office Action dated August 11, 2004 has been received and carefully considered. Reconsideration of the outstanding rejections in the present application is respectfully requested based on the following remarks.

Finality of the Office Action Premature

At page 9 of the Office Action, the Examiner asserted that the Applicants' amendments necessitated the new grounds of rejection in the Office Action and the Office Action therefore was made final. The Applicants respectfully submit that the finality of the Office Action is premature.

As provided by the M.P.E.P.:

> Under present practice, second or any subsequent actions on the merits shall be final, *except where the examiner introduces a new ground of rejection that is neither necessitated by applicant's amendment of the claims* nor based on information submitted in an information disclosure statement filed during the period set forth in 37 CFR 1.97(c) with the fee set forth in 37 CFR 1.17(p). . . . *Furthermore, a second or any subsequent action on the merits in any application* or patent undergoing reexamination proceedings *will not be made final if it includes a rejection, on newly cited art*, other than information submitted in an information disclosure statement . . ., *of any claim not amended by applicant or patent owner in spite of the fact that other claims may have been amended to require newly cited art.*
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> . . .
>
> A second or any subsequent action on the merits in any application or patent involved in reexamination proceedings should not be made final *if it includes a rejection, on prior art not of record, of any claim amended to include limitations which should reasonably have been expected to be claimed.* See MPEP § 904 *et seq.* For example, one would reasonably expect that a rejection under 35 U.S.C. 112 for the reason of incompleteness would be replied to by an amendment supplying the omitted element.

M.P.E.P. § 706.07(a)(emphasis added).

In the response to the Office Action mailed February 19, 2004, claim 13 was amended simply to correct various informalities. Specifically, claim 13 was amended to remove an improperly placed period and to rephrase the phrase "said memory controller to provide *access of system memory to said graphics controller*" as "said memory controller to provide *said*

graphics controller access to system memory" due to the awkwardness of the original phrase. The revised phrase is equivalent to the original phrase and does not introduce new limitations to claim 13 or otherwise modify the scope of claim 13 in any way. Thus, amended claim 13 was not amended for patentability purposes but instead was amended, in effect, for reasons analogous to amendments "expected to be made" in view of 35 U.S.C. § 112. Accordingly, the Applicants respectfully submit that the amendments to claim 13 did not necessitate a new ground of rejection on the part of the Examiner and consequently the finality of the Office Action is premature. Withdrawal of the finality of the Office Action therefore is respectfully requested.

Anticipation Rejection of Claims 13-26 and 29

At page 2 of the Office Action, claims 13-26 and 29 were rejected under 35 U.S.C. § 102(b) as being anticipated by Kou (U.S. Patent No. 5,874,928). This rejection is respectfully traversed.

Claim 13, from which claims 14-20 depend, recites, in part, the limitations of a system comprising a processor to receive a first and a second set of graphics data, an output data bus for providing the first set of graphics data to an external graphics controller, said external graphics controller to generate a first rendered graphics data associated with the first set of graphics data provided using the output data bus and a graphics controller to generate a second rendered graphics data based on the second set of graphics data and provide the second set of rendered graphics data to an external display interface. Thus claim 13 provides for two graphics controllers, one graphics controller that is part of the system (the graphics controller) and a graphics controller that is external to the system (the external graphics controller). Claim 13 further provides that the graphics controller that is part of the system generates a second rendered graphics data based on the second set of graphics data and the external graphics controller generates a first rendered graphics data associated with the first set of graphics data.

With respect to these limitations, the Examiner asserts that

> the first converter 42 converts 116 the serial data stream into a first set of video signals having both an analog portion and a digital portion (receiving a first set and a second set of graphics data). The analog portion is sent 120 on to the CRT display to drive the display (to an external graphics controller, for example the CRT controller 58, Fig. 2), while the digital portion is processed further. . . . The first display is thus driven. To drive the second display, the digital portion of the first set of video signals needs to be converted into a second set of video signals,

> which can be used to drive the second display. This conversion processes preferably begins with the processing (step 124) of the digital portion of the first set of video signals through the second converter 44 to generate a second stream of graphics data, which is appropriate for display by the second display (the LCD). The dithering engine 54 thereafter converts 144 the stream of graphics data from the read buffer into a second set of video signals, and sends 148 the video signals to the flat panel controller 56 (liquid crystal display controller). Finally, the controller 56 sends 152 the video signals to the LCD (to an external display interface) at a rate determined by the rate of the memory clock signal. The second display is thus driven . . . . The examiner make the assumption that components 42, 44, 45, 50, 54 and 56 (Fig. 2) together is the graphics controller, the frame buffer controller 52 is the memory controller . . . .

Office Action, pp. 2-3.

As understood from the Examiner's remarks, it appears that the Examiner considers components 42, 44, 45, 50, 54 and 56 together as disclosing the graphics controller of the system of claim 13 and the CRT controller 58 as disclosing the external graphics controller. As a first issue, the Applicants respectfully submit that the Examiner mischaracterizes the CRT controller 58 as a graphics controller in the context of claim 13. As claim 13 recites, the external graphics controller generates a first *rendered* graphics data associated with the first set of graphics data. In contrast, Kou teaches that "[t]he primary function of converter 42 is to convert the serialized graphics data stream into a first set of video signals. These video signals preferably include an analog portion and a digital portion. *The analog portion is used to drive the CRT display . . .*" and that "in order to properly drive a CRT type of display, control signals are needed in addition to the analog video signals from the first converter [converter 42]" and further teaches that the CRT controller 58 "is the component responsible for generating the control signals, and controlling the overall operation of the display." *Kou*, col. 6, lines 61-65, col. 7, lines 39-41, and col. 7, lines 44-48 (emphasis added). None of these passages or any other passage of Kou disclose or suggest that the CRT controller 58 generates rendered graphic data as is recited by claim 13.

Moreover, one of ordinary skill in the art will appreciate from the teachings of Kou that the first converter 42 provides an analog video signal to the CRT controller 58 to drive a CRT and thus the graphics data is already rendered (i.e., ready to be provided to a display driver) and provided by the converter 42 in the form of the analog video signal to the CRT controller 58. *See Id.* (""[t]he primary function of converter 42 is to convert the serialized graphics data stream

into a first set of video signals."). Thus, Kou fails to disclose or suggest that the CRT controller 58 operates as a graphics controller to generate rendered graphics data. Even if it is assumed, *arguendo*, that the CRT controller 58 operates as a graphics controller (which it does not as detailed above), the CRT controller 58 is not "external" as recited by claim 13. As Figure 2 of Kou demonstrates, the CRT controller 58 is part of the display controller 16 (i.e., a "system") and is thus internal, or part of, the display controller 16. Accordingly, the Applicants respectfully submit that the Office Action fails to establish that Kou discloses or suggests a graphics controller external to a system in addition to a graphics controller that is part of the system, so the Office Action necessarily fails to establish that Kou discloses or suggests the limitations of an output data bus for providing the first set of graphics data to an external graphics controller, said external graphics controller to generate a first rendered graphics data associated with the first set of graphics data provided using the output data bus as recited by claim 13.

As another issue, claim 13 recites the limitations of a processor to receive a first and a second set of graphics data. It is respectfully submitted that the Office Action fails to address how Kou discloses or suggests such a processor. As noted above, it is the Applicants' understanding that the Examiner considers the analog portion and the digital portion of the video signals to be analogous to the first and second set of graphics data, respectively. As depicted by Figure 2 of Kou, the analog portion is provided as a video signal to a CRT and the digital portion is provided to a second converter 44. Thus, Kou fails to disclose or suggest that the analog portion and the digital portion are received by the same component, much less that both are received by a processor. Accordingly, it is respectfully submitted that the Office Action fails to establish that Kou discloses or suggests the limitations of a processor to receive a first set and a second set of graphics data.

Claim 21, from which claims 22-29 depend, recites, in part, the similar limitations of receiving, at a system on a chip, a first set of graphics data and a second set of graphics data, providing the first set of graphics data to an external graphics controller, wherein the external graphics controller generates a first set of rendered graphics data associated with the first set of graphics data and processing, at the system on a chip, the second set of graphics data to generate a second set of rendered graphics data. As noted above, the Office Action fails to establish that Kou discloses or suggests an external graphics controller that generates a set of rendered

graphics data associated with a set of graphics data and consequently fails to disclose or suggest the limitations of providing a set of graphics data to such an external graphics controller as recited by claim 21.

Additionally, claim 21 recites the limitations of the first set of graphics data and the second set of graphics data being received at a system on a chip. The Examiner asserts that "Kou teaches the display controller 16 of FIG. 2 may take one of many forms. It may be implemented in the form of a single integrated circuit device, or it may be implemented with several discrete components on a printed circuit board." *Office Action*, p. 4 (citing col. 11, lines 38-50 of Kou). As noted above, the analog portion and the digital portion (which the Examiner appears to equate to the first and second sets of graphics data of claim 21) of the video signal disclosed in Kou are received by two separate components *external to the video controller 16* and therefore even if the video controller 16 were to be implemented as a system on a chip as the Examiner proposes, the first and second sets of graphics data would not be received by the system on a chip as is recited by claim 21.

In view of the foregoing, it is respectfully submitted that the Office Action fails to establish that Kou discloses or suggests each and every limitation of claims 13 and 21, as well as each and every limitation of claims 14-20, 22-26 and 29 at least by virtue of their dependency from one of claims 13 or 21. Moreover, these claims recite additional limitations neither disclosed nor suggested by Kou.

Accordingly, it is respectfully submitted that the anticipation rejection of claims 13-26 and 29 is improper at this time and withdrawal of this rejection therefore is respectfully requested.

Obviousness Rejection of Claims 1, 3-12 and 27-28

At page 5 of the Office Action, claims 1, 3-8, 11 and 12 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Kou in view of Reddy (U.S. Patent No. 6,075,513). At page 7 of the Office Action, claims 27 and 28 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Kou in view of Narui (U.S. Patent No. 6,313,813). At page 8 of the Office Action, claims 9 and 10 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Kou in view of Reddy and further in view of Narui. These rejections are respectfully traversed.

As noted above, the Office Action fails to establish that Kou discloses or suggests at least the limitations of receiving, at a system on a chip, a first set of graphics data and a second set of graphics data and providing the first set of graphics data to an external graphics controller, wherein the external graphics controller generates a first set of rendered graphics data associated with the first set of graphics data as recited in claim 21, from which claims 27 and 28 depend. The Applicants respectfully submit that the Office Action fails to establish that Narui discloses or suggests at least these limitations. Accordingly, the Office Action fails to establish that the proposed combination of Kou and Narui discloses or suggests each and every limitation of claims 27 and 28 at least by virtue of their dependency on claim 21. Moreover, these claims recite additional limitations neither disclosed nor suggested by the cited references.

Claim 1, from which claims 3 and 5-12 depend, recites, in part, the similar limitations of an embedded system on a chip having a first interface and a second interface, an embedded graphics controller to generate a first rendered graphics data to be displayed on an integrated display, said embedded graphics controller having a first interface coupled to the first interface of said embedded system on a chip and a second interface coupled to the integrated display, an embedded display interface to format a second rendered graphics data for output to a first remote display, said embedded display interface having at least a first input coupled to the second interface of said embedded system on a chip, wherein the embedded system on a chip includes a display controller used to generate said second rendered graphics data and to provide said second rendered graphics data to said embedded display interface. Thus, as with claim 13 discussed above, claim 1 recites the limitations of two components for generating rendered graphics data: the embedded graphics controller to generate the first rendered graphics data and the display controller to generate the second rendered graphics data. As further recited by claim 1, the display controller is part of the embedded system on a chip, whereas the embedded graphics controller is separate from (i.e., external to) the embedded system on a chip.

Even if, *arguendo*, there is motivation to implement the video controller 16 of Kou as a system on a chip as asserted by the Examiner, the proposed combination of the teachings of Kou, Reddy and Narui fails to disclose or suggest a system on a chip having a graphics controller to generate a rendered first set of graphics data as well as a device controller separate from, or external to, the system on a chip to generate a rendered second set of graphics data as recited by claim 1. Accordingly, the Office Action fails to establish that the proposed combination of Kou

and Reddy discloses or suggests each and every limitation of claim 1, as well as each and every limitation of claims 3 and 5-12 at least by virtue of their dependency from claim 1. Moreover these claims recite additional limitations neither disclosed nor suggested by the cited art.

Claim 4 recites, in part, the limitations of an embedded system on a chip having a first interface and a second interface; an embedded graphics controller to generate a first rendered graphics data to be displayed on an integrated display, said embedded graphics controller having a first interface coupled to the first interface of said embedded system on a chip and a second interface coupled to the integrated display; an embedded display interface to format a second rendered graphics data for output to a first remote display, said embedded display interface having at least a first input coupled to the second interface of said embedded system on a chip; and wherein said embedded graphics controller further includes a third interface to interface with a second input of said embedded display interface, and further wherein said embedded graphics controller is further used to provide said first rendered graphics data to said embedded display interface for display on a second remote display. Thus, claim 4 recites the limitations of wherein an embedded graphics controller provides first rendered graphics data to an integrated display as well as a second remote display (via a display interface) and where the display interface formats a second rendered graphics data for display on a first remote display. To summarize, the first rendered set of graphics data is provided for display on both an integrated display and a remote display and the second rendered set of graphics data is provided for display on a remote display, which may be the same or different remote display as the remote display receiving the first rendered graphics data.

The Applicants respectfully submit that the Office Action fails to establish that the proposed combination of the teachings of Kou and Reddy discloses or suggests the provision of the same rendered graphics data for display on both an integrated display and a remote display as well as the provision of a different rendered graphics data on a remote display as recited by claim 4. Accordingly, the Office Action fails to establish that the proposed combination of Kou and Reddy discloses or suggests each and every limitation of claim 4.

In view of the foregoing, it is respectfully submitted that the obviousness rejections of claims 1, 3-12, 27 and 28 are improper at this time and withdrawal of these rejections therefore are respectfully requested.

Addition of New Claims 30 and 31

New claims 30 and 31 have been added. New claim 30 recites the limitations of a method comprising: in a first mode of operation: rendering a first set of graphics data at a graphics controller embedded in a portable device, and providing the rendered first set of graphics data to an LCD integrated with the portable device; and in a second mode of operation: rendering a second set of graphics data at the graphics controller embedded in the portable device, providing the second set of graphics data to the LCD integrated with the portable device, and providing a third set of graphics data to a graphics controller external to the portable device for rendering and display at a display external to the portable device. New claim 31 recites the limitations of a portable device comprising: an integrated LCD; a system on a chip comprising: means for rendering a first set of graphics data; a first output operably coupled to a display interface, the first output operable to provide the rendered first set of graphics data to the display interface for display on a display device external to the portable device; and a second output operable to provide a second set of graphics data; a video controller comprising: an input operably coupled to the second output of the system on a chip to receive the second set of graphics data; means for rendering the second set of graphics data; and an output operably coupled to the integrated LCD to provide the rendered second set of graphics data for display on the integrated LCD. Support for the addition of new claims 30 and 31 may be found in the specification and figures as originally filed.

As noted above, the cited references fail to disclose or suggest the rendering of a first set of graphics data internal to a portable device and the rendering of a second set of graphics data external to the portable device. As these limitations or similar limitations are recited by claims 30 and 31, the cited references necessarily fail to disclose or suggest each and every limitation of new claims 30 and 31.

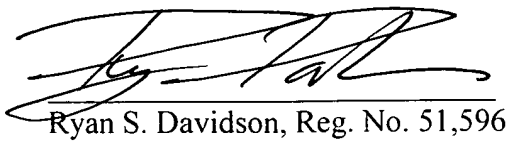
Conclusion

It is respectfully submitted that the present application is in condition for allowance, and an early indication of the same is courteously solicited. The Examiner is respectfully requested to contact the undersigned by telephone at the below listed telephone number in order to expedite resolution of any issues and to expedite passage of the present application to issue, if any comments, questions, or suggestions arise in connection with the present application.

Applicants do not believe that any additional fees are due, but if the Commissioner believes additional fees are due, the Commissioner is hereby authorized to charge any fees which may be required, or credit any overpayment, to Deposit Account Number 50-0441.

Respectfully submitted,

October 11, 2004
Date



Ryan S. Davidson, Reg. No. 51,596
On Behalf Of
J. Gustav Larson, Reg. No. 39,263,
Attorney for Applicants
TOLER, LARSON & ABEL, L.L.P.
5000 Plaza On The Lake, Suite 265
Austin, Texas 78746
(512) 327-5515 (phone) (512) 327-5452 (fax)